FAIRCHILD

SEMICONDUCTOR ™

74LVX32
Low Voltage Quad 2-Input OR Gate

General Description

The LVX32 contains four 2-input OR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

■ Input voltage level translation from 5V to 3V
■ Ideal for low power/low noise 3.3V applications
■ Guaranteed simultaneous switching noise level and dynamic threshold performance

Ordering Code:

Order Number	Package Number	Package Description
74LVX32M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
74LVX32SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVX32MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol
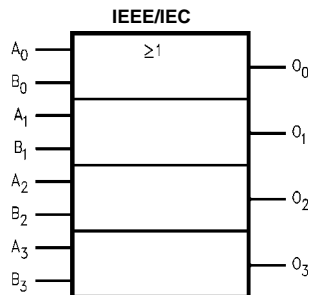
Connection Diagram
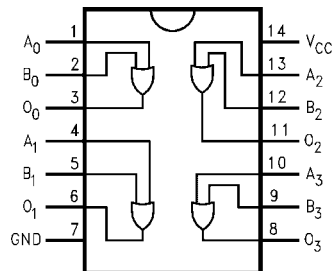
Pin Description

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

DS011604.prf www.fairchildsemi.com

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = −0.5V$	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
$V_O = −0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current	
(I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time ($\Delta t/\Delta V$)	0 ns/V to 100 ns/V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	$T_A = +25°C$			$T_A = −40°C$ to $+85°C$		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Input	2.0	1.5			1.5				
	Voltage	3.0	2.0			2.0		V		
		3.6	2.4			2.4				
V_{IL}	LOW Level Input	2.0			0.5		0.5			
	Voltage	3.0			0.8		0.8	V		
		3.6			0.8		0.8			
V_{OH}	HIGH Level Output	2.0	1.9	2.0		1.9			$V_{IN} = V_{IL}$ or V_{IH}	$I_{OH} = −50$ μA
	Voltage	3.0	2.9	3.0		2.9		V		$I_{OH} = −50$ μA
		3.0	2.58			2.48				$I_{OH} = −4$ mA
V_{OL}	LOW Level Output	2.0		0.0	0.1		0.1		$V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 50$ μA
	Voltage	3.0		0.0	0.1		0.1	V		$I_{OL} = 50$ μA
		3.0			0.36		0.44			$I_{OL} = 4$ mA
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	$V_{IN} = 5.5V$ or GND	
I_{CC}	Quiescent Supply Current	3.6			2.0		20	μA	$V_{IN} = V_{CC}$ or GND	

Noise Characteristics (Note 3)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$		Units	C_L (pF)
			Typ	Limit		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.3	0.5	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.5	V	50
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	3.3		0.8	V	50

Note 3: (Input $t_r = t_f = 3$ ns)

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units	C_L (pF)
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation	2.7		5.8	10.7	1.0	12.5	ns	15
t_{PHL}	Delay Time			8.3	14.2	1.0	16.0		50
		3.3 ± 0.3		4.4	6.6	1.0	7.5		15
				6.9	10.1	1.0	11.5		50
t_{OSLH}	Output to Output	2.7			1.5		1.5	ns	50
t_{OSHL}	Skew (Note 4)	3.3			1.5		1.5		

Note 4: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

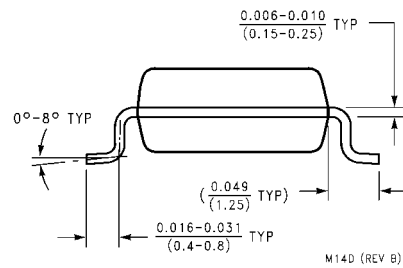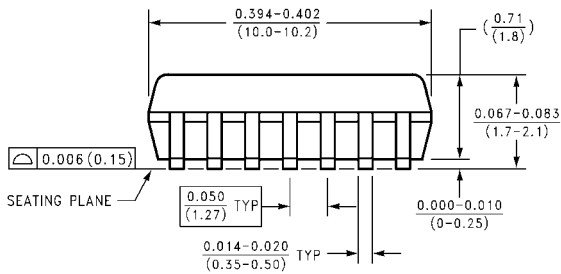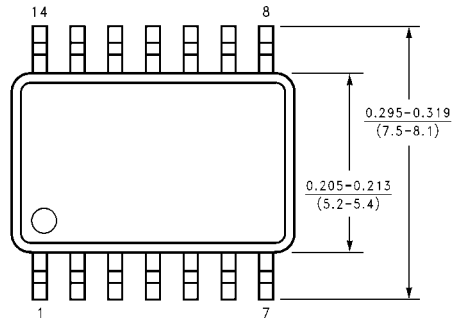| Symbol	Parameter	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units
		Min	Typ	Max	Min	Max	
C_{IN}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)		14				pF

Note 5: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \dfrac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4 \text{ (per Gate)}}$

Physical Dimensions inches (millimeters) unless otherwise noted

0.335 − 0.344
(8.509 − 8.738)

14 13 12 11 10 9 8

0.228 − 0.244
(5.791 − 6.198)

LEAD NO. 1
IDENT

1 2 3 4 5 6 7

30°
TYP

0.010
(0.254) MAX

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) × 45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP

0.004 − 0.010
(0.102 − 0.254)

0.014 − 0.020
(0.356 − 0.508) TYP

M14A (REV H)
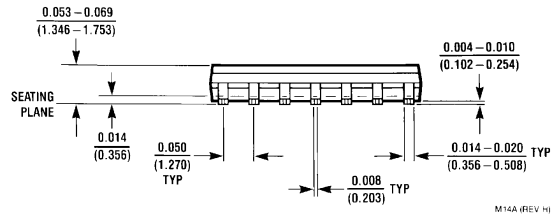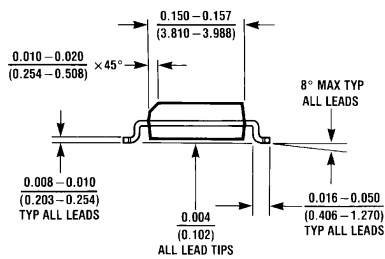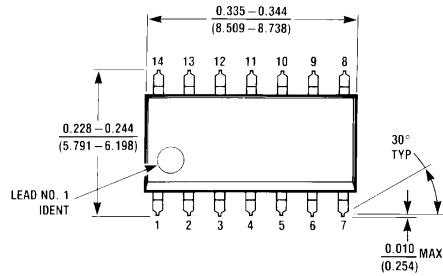
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
Package Number M14A

14   8

1   7

0.295−0.319
(7.5−8.1)

0.205−0.213
(5.2−5.4)

0.394−0.402
(10.0−10.2)

(0.71
(1.8))

0.067−0.083
(1.7−2.1)

0.006 (0.15)

SEATING PLANE

0.050
(1.27) TYP

0.014−0.020
(0.35−0.50) TYP

0.000−0.010
(0−0.25)

0.006−0.010
(0.15−0.25) TYP

0°−8° TYP

(0.049
(1.25) TYP)

0.016−0.031
(0.4−0.8) TYP

M14D (REV B)

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

5.0± 0.1
-A-

0.43 TYP

14   8

6.4

3.2

4.4± 0.1
-B-

1

7

PIN #1 IDENT.

0.2 C B A
ALL LEAD TIPS

7.72

4.16

1.78

0.65   0.42

LAND PATTERN RECOMMENDATION

1.2 MAX

ALL LEAD TIPS

0.1 C

0.90 +0.15 -0.10

-C-

0.10± 0.05

0.65

0.19 - 0.30

0.13 M A B S C S

SEE DETAIL A

0.09-0.20

12.00° TOP & BOTTO

R0.16

R0.31

0°-8°

0.6± 0.1

1.00

GAGE PLANE

0.25

SEATING PLANE

DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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